Office Action Summary	Application No.	Applicant(s)	
	10/658,053	SMITH ET AL.	
	Examiner	Art Unit	
	Jianye Wu	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/31/08 has been entered.

Response to Arguments

1. Applicant's arguments filed on 7/31/2008 regarding U.S.C. 102/103 rejections have been fully considered, but are moot because all independent claims have been amended.

Applicant's arguments to previous claim rejections are moot because all independent claims (including claims 1-3, 10, 17 and 26) have been amended. New ground rejections based on amended claims are presented in this Office Action above.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1-5, 8-9, 10-12, 15-16** are rejected under 35 U.S.C. 102(b) as being anticipated by keenan et al (US 6215789 B1, hereinafter **keenan**).

For **claim 1** and **2**, keenan discloses a method and apparatus for performing time slot switching of synchronous data across an asynchronous packet switch (44 of FIG. 2 and 3) comprising:

(a) converting time-sensitive synchronous serial data related to a plurality of source (data from telephone 38 and 39 of FIG. 3, which is time sensitive) time slots in a time-division multiplexing frame (TDM frame 70 of FIG 5) into synchronous parallel data units (data for CBR Slot 1-4 in 70, FIG. 6 in view of 52 of FIG. 3) in accordance with a synchronous clock signal (system transmitter clock, line 51 of Col. 28) (Notice that (a) is regarding conversion from circuit switched network to packet switched network, which is clearly disclosed either in FIG. 3 or in FIG. 4);

(b) formatting the synchronous parallel data units into at least first subpacket ("CBR slot 1 8 octets" in frame 70 of FIG. 5) and a second subpacket ("CBR slot 2 8 octets" in frame 70 of FIG. 5) in accordance with the synchronous clock signal, the first subpacket and the second subpacket being generated during a first synchronization interval of the synchronous clock signal (each subacket is transmitted in the given time slot as shown in FIG. 5); the first subpacket being associated with a first source time slot in the time-drivision multiplexing frame and comprsing an ingress queue identifier (identifier of TX TDM flow Queue 58 of FIG. 3) and a first destination time slot identifier (slot number of CBR slot 1) used for and the second subpakcet being associated with a

second source time slot (slot number of slot 2) in the time division multiplexing frame and comprising the same ingress queue identifier (both subackets are in the same queue 58 of FIG. 3) and a second destination time slot identifier (slot number of CBR slot 2, FIG. 5);

(c) generating a packet (70 of FIG. 5) including the first subpacket sharing the same ingress queue identifier, including the first subpacket and the second subpacket, the packet comprising a synchronization tag identifying the synchronization interval in which the first subpacket and the second subpacket were formatted (slot number of CBR slot in FIG. 5);

(d) asynchronously transmitting the packet across an asynchronous packet switch (Lines 27-30, Col. 28; or packets transmitted between Ethernet network switches such as traffic between 54 and 56, notice that the medium connecting switches is asynchronous); and

(e) extracting the subpackets from the packet and storing the subpackets in a first buffer and a second buffer (receiving data buffers 58 of FIG. 3 in view of FIG. 5 where subpackets are extracted from frame 70), the first buffer being associated with the first destination time slot (data in CBR slot 1 of 70) and the second buffer (data in CBR slot 2 of 70) being associated with the second destination time slot, the arrangement of subpackets within the buffers being determined by the first synchronization interval during which the subpacket was generated plus a known fixed delay offset (line 61-65, Col. 29, CBR transmission delay between two time slots is known).

For **claim 3** and **10**, keenan discloses a method and an apparatus for transferring data comprising:

(a) packetizing a plurality of time-sensitive synchronous serial data source (data sources from telephone 38 and 39 of FIG. 3, which are time sensitive) related to a plurality of source time slots in a time-division multiplexing frame (TDM frame 70 of FIG 5) into first subpacket and second subpacket during a first synchronous parallel data units (data for CBR Slot 1-4 in 70, FIG. 6 in view of 52 of FIG. 3), in accordance with a synchronous clock signal (system transmitter clock, line 51 of Col. 28) (Notice that (a) is regarding conversion from circuit switched network to packet switched network, which is clearly disclosed either in FIG. 3 or in FIG. 4);

(b) asynchronously transmitting at least the first subpacket ("CBR slot 1 8 octets" in frame 70 of FIG. 5) and a second subpacket ("CBR slot 2 8 octets" in frame 70 of FIG. 5) in accordance with the synchronous packet switch (Ethernet switch system 44, FIG. 3);

(c) reconverting the first subpacket and second subpacket into synchronous data streams (data frame 70 of FIG.3) comprising a first destination time slot and a second data stream associated with a second destination time slot, and the first subpacket and the second subpacket reconverted during a second synchronization interval having a known a known fixed delay to the first synchronization interval (line 61-65, Col. 29, CBR transmission delay between two time slots is known).

As to **claim 4** and **11**, keenan discloses claim 3 and 10, wherein (a) comprises:

(a1) converting the synchronous serial data streams into synchronous parallel

data units (data units for CBR slot 1-4 in 70 of FIG. 6, the data units are considered as parallel since they are in the same frame and are sent at the same time).

As to **claim 5** and **12**,, keenan discloses claim 4 and 11, wherein (a) comprises:

(a2) formatting the synchronous parallel data units into a respective subpacket during a first synchronization interval (CBR data part of 70 of FIG. 6).

As to **claim 8** and **15**, keenan discloses the method of claim 3 and 10 wherein (c) comprises:

(c1) extracting the subpackets from the packet (Line 41-44, col. 28), and

(c2) storing the subpackets into a plurality of buffers, each of the buffers buffers (TDM Flow Queue, Line 43, col. 28) associated with a destination time slot, the arrangement of subpackets within the buffers being determined by a value representing the first synchronization interval plus a fixed delay offset (128μs, Line 46 of Col. 28).

As to **claim 9** and **16**, keenan discloses claim 8 and 15, wherein (c) comprises:

(c3) reading the subpackets from the buffers as a plurality of parallel data units (data for CBR Slot 1-4 in 70, FIG. 6, with data for each time slot be considered as a data unit); and

(c4) converting the parallel data units into synchronous serial data streams (data from 61 to 52 in FIG.3).

3. **Claims 17-19** are rejected under 35 U.S.C. 102(e) as being anticipated by Ethridge et al. (US 6466572, hereinafter **Ethridge**).

For **claim 17**, Ethridge discloses an apparatus comprising:

(a) an asynchronous switch (66 of Fig. 5);

(b) a plurality of circuit server modules coupled to the asynchronous switch, the server modules comprising (94 of Fig. 5):

(i) a time division multiplex interface (78 or 82 of Fig 4); and

(ii) data adaptation logic (78 or 82 of Fig 4); and

(c) a source of synchronous clock signals (e.g., system clock, 138 of Fig. 7) coupled to each of the circuit server modules, the synchronous clock signals defining a plurality of synchronization intervals (in fact, circuit server modules inherently associated with a source of synchronous clock signals, which is a common knowledge in the art); the circuit server modules (54 of Fig. 4) configured to perform synchronous time slot switching of synchronous data (data from 56 of Fig. 4) across the asynchronous switch (66 of Fig. 4).

As to **claim 18**, Ethridge discloses the apparatus of claim 17 wherein the time division multiplex interface comprises: serial to parallel conversion logic for converting synchronous serial data streams into parallel data units (60 of Fig. 4).

As to **claim 19**, Ethridge discloses the apparatus of claim 17 further comprising: parallel-to-serial conversion logic for converting a plurality of parallel data units into synchronous serial data streams (60 of Fig. 4).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the

subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 6-7, 13-14 and **26** are rejected under 35 U.S.C. 103(a) as being unpatentable over keenan et al (US 20030072269, hereinafter **keenan**) in view of Luby et al., "Reliable Multicast Transport Building Block: Multirate Congestion Control", draft-ietf-rmt-bb-mrcc-00.txt, July 2000, hereinafter Luby.

As to **claim 6**, keenan discloses the method of claim 5 wherein (b) comprises:

(b1) generating a packet (70 of FIG. 6) from a plurality of subpackets (the subpacket for CBR data and the subpacket contain packet data in 70 of FIG. 6),

keenan is silent on the packet including data identifying the first synchronization interval during which the subpackets were formatted from the synchronous parallel data units, and a destination time slot identifier associated with each subpacket.

Luby teaches including time slot information (places into each packet the time slot index, Line 10 of Page 8) and other information (Line 7 of Page 8) into each packet.

Keenan and Luby teach the same art, one skilled in the art would be motivated to combine them together for the benefit of providing more information for the receiver.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to to combine them together for the benefit of providing more information for the receiver.

As to **claim 7**, keenan discloses the method of claim 6 wherein (b) comprises:

(b2) asynchronously transmitting the subpackets through an asynchronous packet switch (44 of FIG. 2-3) as part of the packet (Lines 27-30, Col. 28).

As to **claims 13-14**, they the corresponding apparatus claims of claim 6-7, therefore, are rejected for the same reason explained above.

For **claim 26**, Keenan discloses a memory for storing data to be processed by a data processing system including an asynchronous switch, the memory comprising:

a data structure stored in the memory and usable to perform time slot switching of data (58 of FIG. 3), the data structure comprising:

a plurality of subpackets (FIG. 8), comprising at least first subpacket ata in (CBR slot 1, FIG. 5) associated with a first source time slot (CBR slot 1, FIG. 5) in a time-division multiplexing frame (frame 70 in FIG. 5) and comprising an ingress queue

identifier (identifier of queue 58, FIG. 3) of a first destination time slot (time slot of CBR slot 1) identifier (slot number) and a second subpacket (CBR slot 2, FIG. 5) associated with a second source time slot (slot number of CBR slot 2, FIG. 5) in a time-division multiplexing frame (frame 70, FIG. 5) and comprising the same ingress qaueue identifier and a second destination slot identifier, the plurality of supackets containing parallel data derived from a synchronous serial data stream (data for CBR Slot in 72 of FIG. 8), each subpacket constructed during a common synchronization interval;

Keenan is silent on a synchronization tag identifying the common synchronization interval during which the plurality of subpackets were constructed; data identifying the number of subpackets contained within the data structure; and context data associated with each one of the plurality of subpackets, the context data including a destination time slot identifier corresponding to the source time slot associated with the subpackets.

In the same field of endeavor, Luby teaches a synchronization tag (time slot index, Line 10 of Page 8) identifying the common synchronization interval during which the plurality of subpackets were constructed; and other information (Line 7 of Page 8) into each packet; though Luby does not explicitly specify the other information comprising the number of subpackets contained within the data structure and context data, but he suggests implicitly that the packet may contain any data needed.

Keenan and Luby teach the same art, one skilled in the art would be motivated to combine them together for the benefit of providing more information for the receiver.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine them together for the benefit of providing more

information for the receiver.

5. **Claims 20-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ethridge as applied to claim 20 above, and further in view of keenan and Luby.

As to **claim 20**, Ethridge discloses the apparatus of claim 18 wherein the data adaptation layer comprises:

Ethridge **is silent on** an ingress data memory coupled to the time division multiplexed interface; an ingress context memory; and subpacket construction logic for constructing in the ingress data memory a plurality of subpackets during one of the synchronization intervals, each subpacket associated with a source time slot and containing parallel data derived from a synchronous serial data stream received through the time division multiplexed interface subpacket.

Keenan discloses an ingress data memory (TDM Flow Queue , lines 14-15, Col. 28) coupled to the time division multiplexed interface (38 or 39 of FIG. 3); an ingress context memory (Timing and Control logic, line 18 of Col. 28; or 46 of FIG. 3); and subpacket construction logic (54 of FIG. 3) for constructing in the ingress data memory a plurality of subpackets during one of the synchronization intervals (72 of FIG. 7), each subpacket associated with a source time slot and containing parallel data derived from a synchronous serial data stream (data in CBR Slot, 72 of FIG. 7) received through the time division multiplexed interface subpacket.

Since Ethridge and Keenan teach the same art, one skilled in the art would have motivated to combine them together.

Therefore, it would have been obvious to a person of ordinary skill in the art at

the time of the invention to combine Ethridge and Keenan due to obvious industry expedient.

As to **claim 21**, Ethridge discloses the apparatus of claim 20.

Ethridge **is silent on** wherein the ingress context memory stores context data associated with a subpacket, the context data comprising a destination time slot identifier and a queue identifier associated with a subpacket.

Keenan discloses the context data **comprising** destination time slot information (CBR slot 1-4, FIG. 5); Luby further discloses the destination time slot identifier (*time slot index*, line 10 of Page 8) and other information (Line 7 of Page 8) into each packet, as also suggested by Ethridge (Lines 24-27 of Col 13).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to include the context data comprising a destination time slot identifier and a queue identifier for the benefit of providing more detailed information for the receiver.

As to **claim 22**, Ethridge, Keenan and Luby in combination disclose the apparatus of claim 21, Keenan further discloses the data adaptation layer comprises: an ingress queue (TX TDM Flow Queue, 58 of FIG. 3) coupled to the asynchronous switch (59 of FIG. 3); and packet construction logic for constructing in the ingress queue a packet including a plurality of subpackets and the respective context data associated with each subpacket (61 of FIG. 3).

As to **claim 23**, Ethridge, Keenan and Luby in combination disclose the apparatus of claim 22, Luby further discloses wherein the packet further comprises data

identifying the synchronization interval during which the subpackets contained therein were constructed (*time slot index*, line 10 of Page 8).

6. **Claims 24-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ethridge in view of keenan.

As to **claim 24**, Ethridge discloses the apparatus of claim 17.

Ethridge **is silent on** wherein the data adaptation layer further comprises: an egress data memory having a plurality of playout buffers associated with a plurality of destination time slots; and depacketizing logic for receiving a packet form the asynchronous switch and for storing subpackets contained therein into the plurality of playout buffers in the egress data memory.

Keenan discloses an egress data memory having a plurality of playout buffers associated with a plurality of destination time slots (RX TDM Flow Queue, 58 of FIG. 3); and depacketizing logic for receiving a packet form the asynchronous switch and for storing subpackets contained therein into the plurality of playout buffers in the egress data memory (46 of FIG. 3)

Ethridge and Keenan teach in the same art. One skilled in the art would have been motivated to combine them for the benefit of providing more functions for users.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Ethridge and Keenan for the benefit of providing more functions for users.

As to **claim 25**, Ethridge and Keenan in combination discloses the apparatus of claim 24 Keenan further discloses wherein the data adaptation layer further comprises:

playout logic (64 of FIG. 3) for synchronously supplying parallel data (TX TDM Flow Queue, 58 of FIG. 3 and 70 of FIG. 6) from the playout buffers (64 of FIG. 3) to the time division multiplexed interface (61 of FIG. 3).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jianye Wu whose telephone number is (571)270-1665. The examiner can normally be reached on Monday to Friday, 8am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (571)272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jianye Wu/

Examiner, Art Unit 2616

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